

IN THE CLAIMS:

Please cancel claims 1 and 2.

13. (Canceled).

14. (Canceled).

15. The semiconductor wafer of claim 3, wherein each chip section has a center and a periphery and said interconnection layers extend from said periphery toward said center, and wherein the plurality of chip electrodes are positioned on said periphery.

16. The semiconductor wafer of claim 4, wherein each chip section has a center and a periphery and said interconnection layers extend from said periphery toward said center, and wherein the plurality of chip electrodes are positioned on said periphery.

17. (Canceled).

18. (Canceled).

19. (Canceled).

20. (Canceled).

21. (Canceled).

22. (Canceled).

23. (Canceled).

24. (Canceled).

25. A semiconductor wafer, including:

a plurality of the sections defined thereon by scribe lines, each chip section having bump electrodes formed simultaneously thereon, the scribe lines for separating the chip sections from each other without dividing bump electrodes thereon, said chip section including:

a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes,
said chip section having a center and a periphery and said interconnection layers extend from said periphery toward said center,

wherein said bump electrodes are arranged in a grid array.

26. A semiconductor wafer, including:

a plurality of chip sections defined theron by scribe lines,

each chip section having:

bump electrodes formed simultaneously theron; a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes,
said chip section having a center and a periphery and said interconnection layers extend from said periphery toward said center,

wherein said bump electrodes are arranged in a grid array.

27. The semiconductor wafer of claim 3, wherein said bump electrodes are arranged in a grid array.

28. The semiconductor wafer of claim 4, wherein said bump electrodes are arranged in a grid array.

29. A semiconductor wafer, including:

a plurality of the sections defined thereon by scribe lines, each chip section having bump electrodes formed simultaneously thereon, the scribe lines for separating the chip sections from each other without dividing bump electrodes thereon, said chip section including:

a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes,

said chip section having a center and a periphery and said interconnection layers extend from said periphery toward said center,

wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.

30. A semiconductor wafer, including:

a plurality of chip sections defined theron by scribe lines,

each chip section having:

bump electrodes formed simultaneously theron; a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes,

said chip section having a center and a periphery and said interconnection layers extend from said periphery toward said center,

wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.

31. The semiconductor wafer of claim 3, wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.

32. The semiconductor wafer of claim 4, wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.